ICmic
IC MICROSYSTEMS

12/10/8-Bit Low Power Dual DACs With Serial Interface and Voltage Output

FEATURES

- 12/10/8-Bit Dual DAC in 08 Lead MSOP Package
- Ultra-Low Power Consumption
- Guaranteed Monotonic
- Wide Output Voltage Swing
- Three-wire SPI/QSP and Microwire Interface Compatible
- Three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z)
- Schmitt-Triggered Inputs for Direct Interfacing to Opto-couplers

APPLICATION

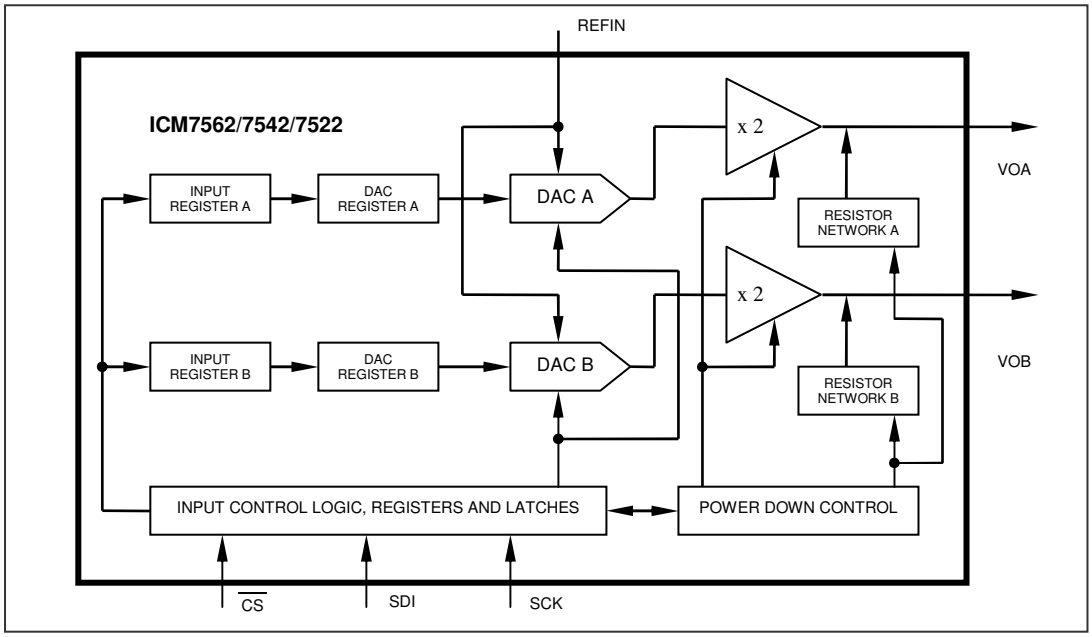
- Battery-Powered Applications
- Industrial Process Control
- Digital Gain and Offset Adjustment

OVERVIEW

The ICM7562, ICM7542 and ICM7522 are 12-Bit, 10-Bit and 8-Bit Voltage Output, Low Power, Dual DACs respectively, with guaranteed monotonic behavior. These DACs are available in 08 Lead MSOP package. They have three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z) as additional safety feature for applications that drive transducers or valves. The operating supply range is 2.7V to 5.5V.

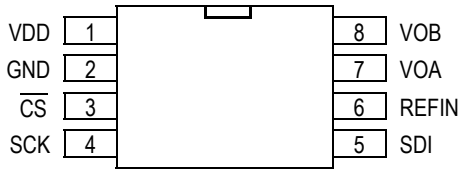
The input interface is an easy to use three-wire SPI, QSPI and Microwire compatible interface. The DAC has Schmitt-Triggered Inputs for Direct Interfacing to Opto-couplers easily.

BLOCK DIAGRAM



PACKAGE

08 Lead MSOP



TOP VIEW

PIN DESCRIPTION (8 Lead MSOP)

Pin	Name	I/O	Description
1	VDD	I	Supply Voltage
2	GND	I	Ground
3	$\overline{CS}$	I	Active Low Chip Select (CMOS)
4	SCK	I	Serial Clock Input (CMOS)
5	SDI	I	Serial Data Input (CMOS)
6	REFIN	I	Reference Voltage Input to DAC A-B
7	VOA	O	DAC A Output Voltage
8	VOB	O	DAC B Output Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (SCK, SDI , $\overline{CLR}$, $\overline{CS}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Operating Temperature Range	Package
ICM7562	-40 °C to 85 °C	08-Lead MSOP
ICM7542	-40 °C to 85 °C	08-Lead MSOP
ICM7522	-40 °C to 85 °C	08-Lead MSOP

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
ICM7562						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7542						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7522						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
STATIC ACCURACY						
GE	Gain Error				±0.5	% of FS
OE	Offset Error				±25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7	5	5.5	V
I_{DD}	Supply Current	Full Scale at VDD=5..5		125	200	µA
		Full Scale at VDD=3.6		100	190	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Vout	Output Voltage Range	(Note 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
Rout	Output Impedance	Power-Down at 1 K Ohm	0.9	1	1.1	KΩ
		Power-Down at 100 K Ohm	90	100	110	KΩ
	Output Line Regulation	V_{DD}=2.7 V to 5.5 V	-3.0	0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	2.4			V
V_{IL}	Digital Input Low	(Note 2)			0.8	V
	Digital Input Leakage				5	

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			2		V/µs
	Settling Time			8		µs
	Mid-scale Transition Glitch Energy			40		nV-S

Note 1: Linearity is defined from code 110 to 3990 (ICM7562)
Linearity is defined from code 16 to 1023 (ICM7542)
Linearity is defined from code 4 to 255 (ICM7522)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	SCK Cycle Time	(Note 2)	30			ns
t_2	Data Setup Time	(Note 2)	10			ns
t_3	Data Hold Time	(Note 2)	10			ns
t_4	SCK Falling edge to $\overline{CS}$ Rising	(Note 2)	0			ns
t_5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	15			ns
t_6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns

SERIAL INTERFACE TIMING AND OPERATION DIAGRAM

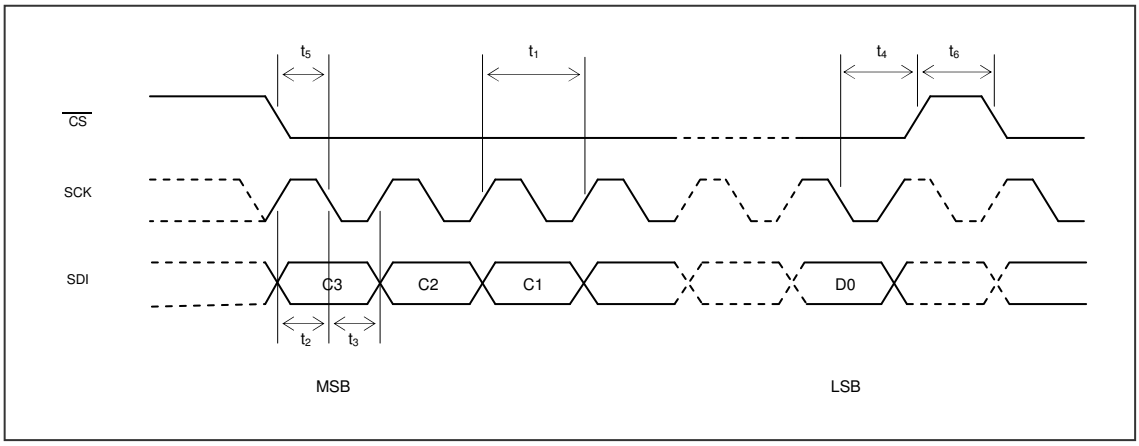


Figure 1. Serial Interface Timing Diagram

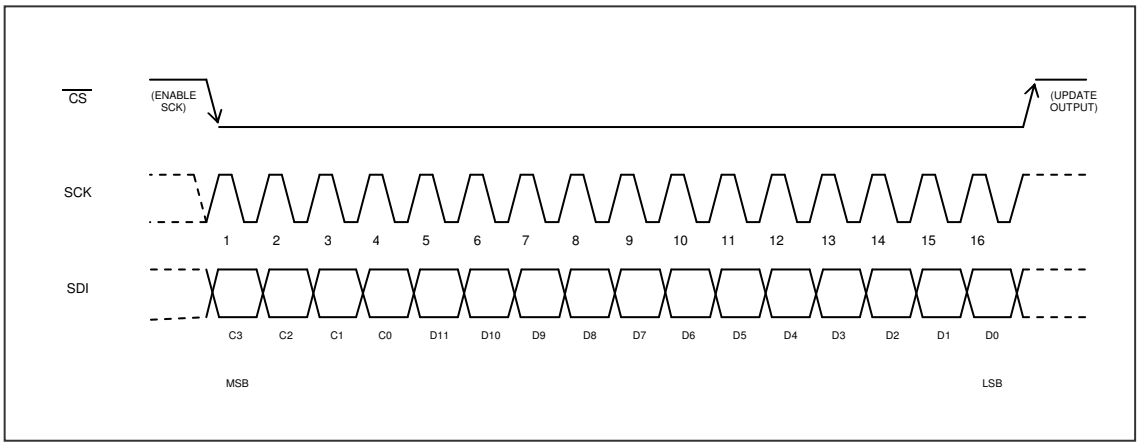


Figure 2. Serial Interface Operation Diagram

CONTENTS OF INPUT SHIFT REGISTER

DEVICE	BIT	CONTROL WORD				DATA WORD											
		MSB															LSB
ICM7562	12	C3	C2	C1	C0	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ICM7542	10	C3	C2	C1	C0	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	A1	A0
ICM7522	8	C3	C2	C1	C0	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	A3	A2	A1	A0

Figure 3. Contents of Input Shift Register

C3	C2	C1	C0	DATA (D11~D0) (D9~D0) (D7~D0)	DAC	FUNCTION
0	0	0	0	Data	A	Input Register transparent, data shifted to DAC register directly, VOA updated
0	0	0	1	Data	B	Input Register transparent, data shifted to DAC register directly, VOB updated
0	1	0	0	Data	A	Data Shifted to Input Register, VOA unchanged
0	1	0	1	Data	B	Data Shifted to Input Register, VOB unchanged
1	0	0	0	Data	A	Data Shifted from Input Register to DAC register, VOA updated
1	0	0	1	Data	B	Data Shifted from Input Register to DAC register, VOB updated
1	1	0	0	Data	All	Input Registers transparent, data shifted to DAC register directly, All VOUT updated
1	1	0	1	Data	All	Data Shifted to Input Registers, All VOUT unchanged
1	1	1	0	Data	All	Data Shifted from Input Registers to DAC registers, All VOUT updated
1	1	1	1	Data	All	Please see Power Down Mode Control Table

Table 1. Serial Interface Input Word

CONTROL				DATA						DAC	FUNCTION
C3	C2	C1	C0	D11~D5 D9~D3 D7~D1	D4 D2 D0	D3 D1 A3	D2 D0 A2	D1 A1 A1	D0 (7562) A0 (7542) A0 (7522)		
1	1	1	1	X	0	X	0	0	0	A	DAC O/P, wakeup
1	1	1	1	X	0	X	0	0	1	A	Floating Output
1	1	1	1	X	0	X	0	1	0	A	Output is terminated with 1KΩ
1	1	1	1	X	0	X	0	1	1	A	Output is terminated with100 KΩ
1	1	1	1	X	0	X	1	0	0	B	DAC O/P, wakeup
1	1	1	1	X	0	X	1	0	1	B	Floating Output
1	1	1	1	X	0	X	1	1	0	B	Output is terminated with 1KΩ
1	1	1	1	X	0	X	1	1	1	B	Output is terminated with100 KΩ
1	1	1	1	X	1	X	0	0	0	All	DAC O/P, wakeup
1	1	1	1	X	1	X	0	0	1	All	Floating Output
1	1	1	1	X	1	X	0	1	0	All	Output is terminated with 1KΩ
1	1	1	1	X	1	X	0	1	1	All	Output is terminated with100 KΩ

Table 2. Power Down Mode Control

DETAILED DESCRIPTION

The ICM7562 is a 12-bit voltage output Dual DAC. The ICM7542 is the 10-bit version of this family and the ICM7522 is the 8-bit version. These devices have a 16-bit data-in shift register and each DAC has a double buffered input.

This family of DACs has a guaranteed monotonic behavior. The operating supply range is from 2.7V to 5.5V.

Reference Input

The reference input accepts positive DC and AC signals. The voltage at REFIN sets the full-scale output voltage of both the DACs. The reference input voltage range is from 0 to VDD-1.5V. The impedance at this pin is very high (greater than 10 M Ohm). Each DACs output amplifier is configured in a gain of 2 configuration. This means that the full-scale output of each DAC will be 2x V_{REF}. To determine the output voltage for any code, use the following equation.

$$V_{OUT} = 2 \times (V_{REF} \times (D / (2^n)))$$

Where D is the numeric value of DAC's decimal input code, V_{REF} is the reference voltage and n is number of bits, i.e. 12 for ICM7562, 10 for ICM7542 and 8 for ICM7522.

Output Buffer Amplifier

The Dual DAC has 2 output amplifiers connected in a gain of 2 configuration. These amplifiers have a wide output voltage swing. The actual swing of the output amplifiers will be limited by offset error and gain error. See the Applications Information section for a more detailed discussion.

The output amplifier can drive a load of 2.0 K Ω to V_{DD} or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 8 μs and it dissipates about 100 μA with a 3V supply voltage.

Serial Interface and Input Logic

This dual DAC family uses a standard 3-wire connection compatible with SPI/QSPI and Microwire interfaces. Data is always loaded in 16-bit words which consist of 4 address and control bits (MSBs) followed by 12 bits (see Figure .3). The last 5 bits of this 12 bit word are also used for power down control (see tables 1 and 2). Each DAC is double buffered with an input latch and DAC latch.

Serial Data Input

SDI (Serial Data Input) pin is the data input pin for all DACs. Data is clocked in on the falling edge of SCK which has a Schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The Chip Select pin which is the 3rd pin of 8 lead MSOP package is active low. This pin frames the input data for synchronous loading and must be low when data is being clocked into the part. There is an onboard counter on the clock input and after the 16th clock pulse the data is automatically transferred to a 16-bit input latch and the 4 bit control word (C3~C0) is then decoded and the appropriate DAC is updated or loaded depending on the control word (see Table 1). Chip Select pin must be pulled high (level-triggered) and back low for the next data word to be loaded in. This pin also disables the SCK pin internally when pulled high.

The DAC has a double-buffered input with an input latch and a DAC latch. The DAC output will swing to its new value when data is loaded into the DAC latch. The user has three options: loading only the input latch, updating the DAC with data previously loaded into the input latch or loading the input latch and updating the DAC at the same time with a new code. The actual data that gets loaded into the DAC latch is D11~D0 for the ICM7562, D9~D0 for the ICM7542 and D7~D0 for the ICM 7522.

Power-Down Mode

The DAC have three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z) as additional safety feature for applications that drive transducers or valves. The power down can be done with loading the control word with 1111 (C0 to C3). Tthe selection of the Output Impedance of DAC is controlled by the last 5 bits. See Table 1 and Table 2 for details of operation of this function.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage output will go to ground.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD}. However, offset and gain error limit this ability. Figure 4 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 5 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

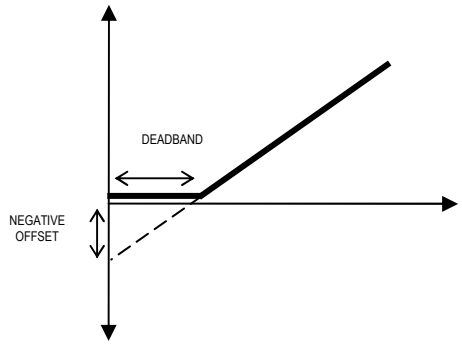


Figure 4. Effect of Negative Offset

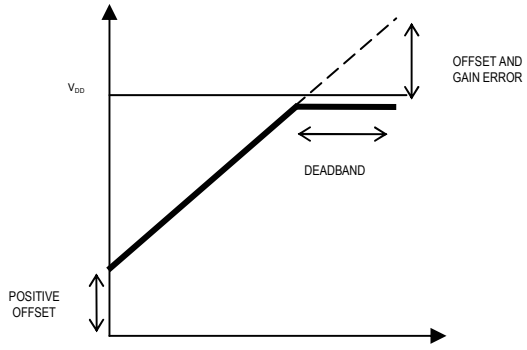
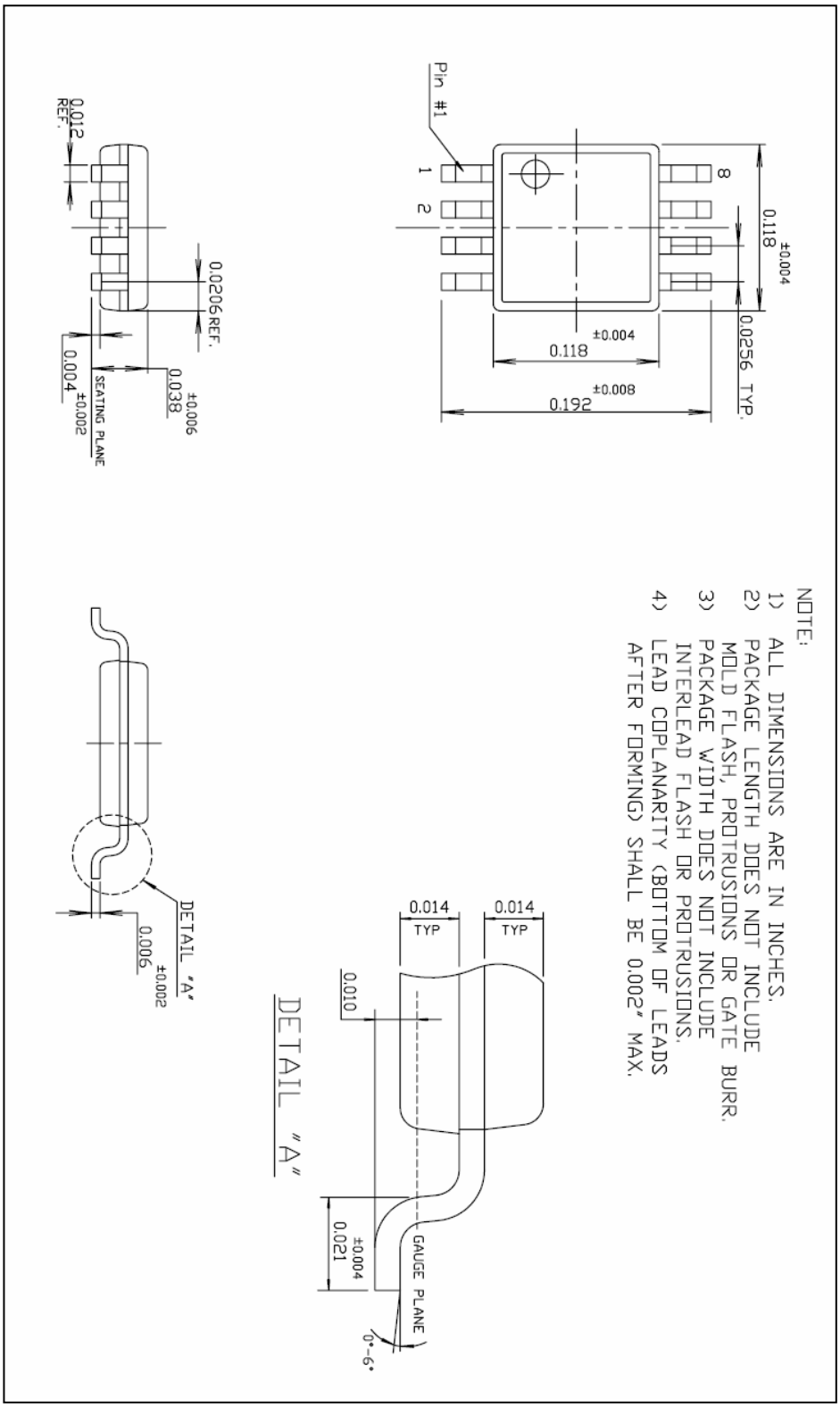


Figure 5. Effect of Gain Error and Positive Offset

PACKAGE INFORMATION

8 Lead MSOP



ORDERING INFORMATION